PTFA081501E
PTFA081501F

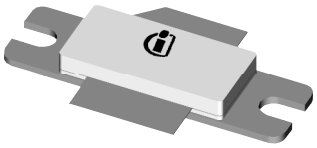
green Product

Thermally-Enhanced High Power RF LDMOS FETs
150 W, 864 – 900 MHz

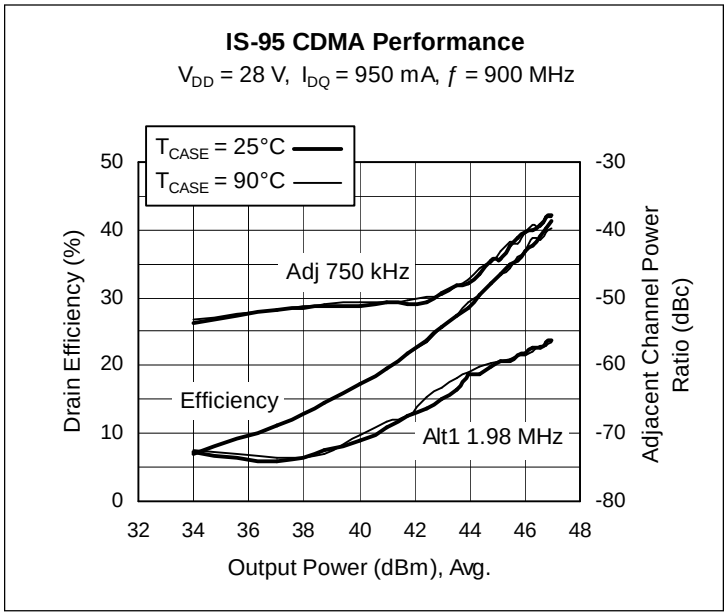
Description

The PTFA081501E and PTFA081501F are thermally-enhanced, 150-watt, internally matched *GOLDMOS*® FETs intended for ultra-linear applications. They are characaterized for CDMA and CDMA2000 operation from 864 to 900 MHz. Thermally-enhanced packages provide the coolest operation available. Full gold metallization ensures excellent device lifetime and reliability.

PTFA081501E
Package H-30248-2



PTFA081501F
Package H-31248-2



Features

- Thermally-enhanced packages, Pb-free and RoHS-compliant
- Broadband internal matching
- Typical CDMA2000 performance at 900 MHz, 28 V
  - Average output power = 35 W
  - Linear Gain = 18 dB
  - Efficiency = 34%
  - Adjacent channel power = –50 dBc
- Typical CW performance, 900 MHz, 28 V
  - Output power at P–1dB = 165 W
  - Efficiency = 62%
- Integrated ESD protection: Human Body Model, Class 2 (minimum)
- Excellent thermal stability, low HCI drift
- Capable of handling 10:1 VSWR @ 28 V, 170 W (CW) output power

RF Characteristics

CDMA2000 3-Carrier Measurements (not subject to production test—verified by design/characterization in Infineon test fixture)

V_{DD} = 28 V, I_{DQ} = 950 mA, P_{OUT} = 35 W average, f = 900 MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	G_{ps}	—	18	—	dB
Drain Efficiency	η_D	—	34	—	%
Adjacent Channel Power Ratio	ACPR	—	–50	—	dBc

All published data at T_{CASE} = 25°C unless otherwise indicated

ESD: Electrostatic discharge sensitive device—observe handling precautions!

RF Characteristics (cont.)

Two-tone Measurements (tested in Infineon test fixture)

V_{DD} = 28 V, I_{DQ} = 950 mA, P_{OUT} = 150 W PEP, f = 900 MHz, tone spacing = 1 MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	G_{ps}	17	18	—	dB
Drain Efficiency	η_D	44	46	—	%
Intermodulation Distortion	IMD	—	–30	–28	dBc

DC Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_{DS} = 10 mA	$V_{(BR)DSS}$	65	—	—	V
Drain Leakage Current	V_{DS} = 28 V, V_{GS} = 0 V	I_{DSS}	—	—	1.0	µA
	V_{DS} = 63 V, V_{GS} = 0 V	I_{DSS}	—	—	10.0	µA
On-State Resistance	V_{GS} = 10 V, V_{DS} = 0.1 V	$R_{DS(on)}$	—	0.07	—	Ω
Operating Gate Voltage	V_{DS} = 28 V, I_{DQ} = 950 mA	V_{GS}	2.0	2.48	3.0	V
Gate Leakage Current	V_{GS} = 10 V, V_{DS} = 0 V	I_{GSS}	—	—	1.0	µA

Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	V
Gate-Source Voltage	V_{GS}	–0.5 to +12	V
Junction Temperature	T_J	200	°C
Total Device Dissipation	P_D	449	W
Above 25°C derate by		2.56	W/°C
Storage Temperature Range	T_{STG}	–40 to +150	°C
Thermal Resistance (T_{CASE} = 70°C, 150 W CW)	$R_{\theta JC}$	0.39	°C/W

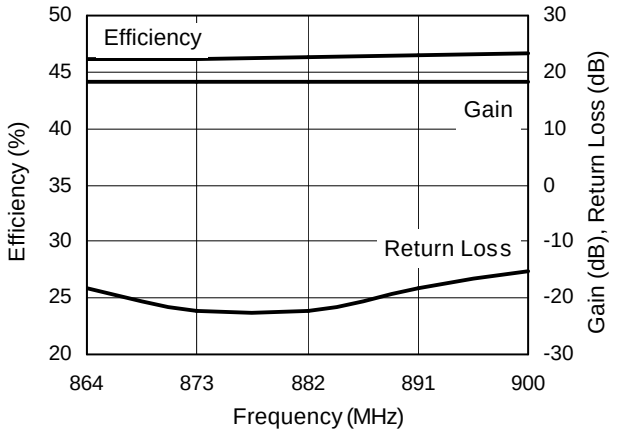
Ordering Information

Type	Package Outline	Package Description	Marking
PTFA081501E	H-30248-2	Thermally-enhanced slotted flange, single-ended	PTFA081501E
PTFA081501F	H-31248-2	Thermally-enhanced earless flange, single-ended	PTFA081501F

Typical Performance (data taken in a production test fixture)

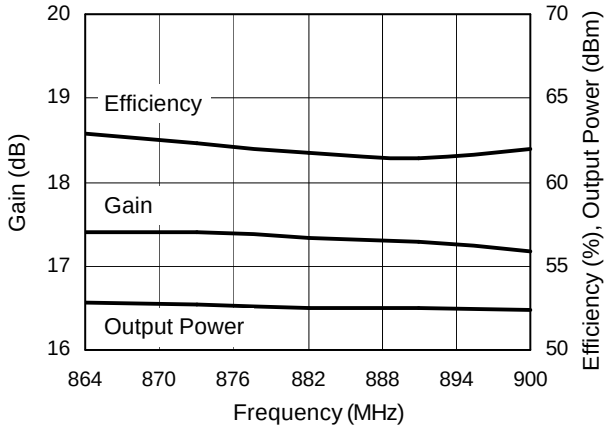
Linear Broadband Performance

V_{DD} = 28 V, I_{DQ} = 950 mA, P_{OUT} Avg. = 48.75 dBm



Broadband CW Performance

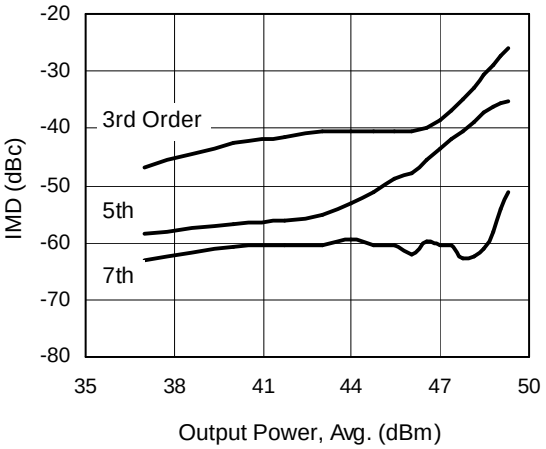
V_{DD} = 28 V, I_{DQ} = 950 mA, P_{OUT} = P–1dB



Intermodulation Distortion vs. Output Power

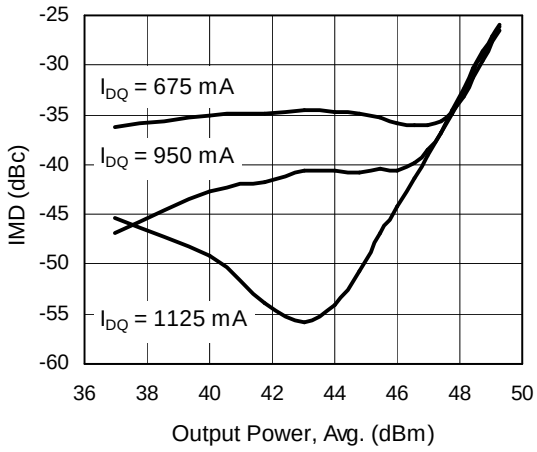
(as measured in a broadband circuit)

V_{DD} = 28 V, I_{DQ} = 950 mA, f_1 = 899 MHz, f_2 = 900 MHz



IM3 vs. Output Power at Selected Biases

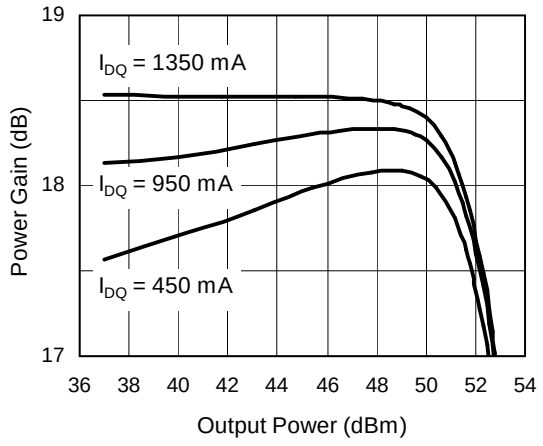
V_{DD} = 28 V, f_1 = 899 MHz, f_2 = 900 MHz



Typical Performance (cont.)

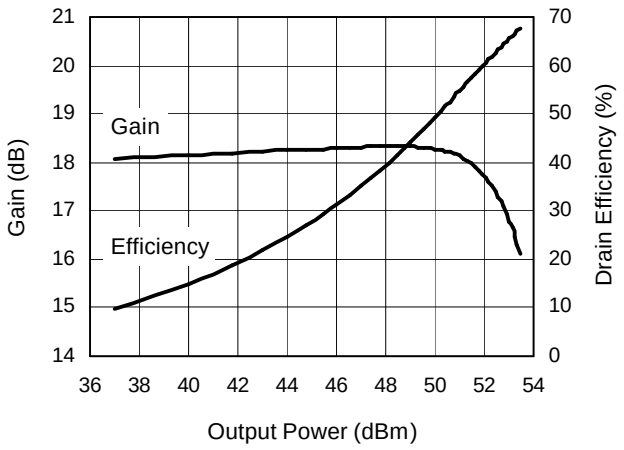
Power Sweep

V_{DD} = 28 V, f = 900 MHz



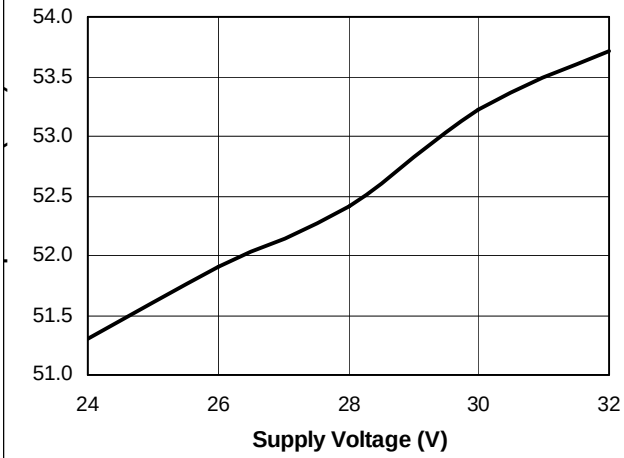
Gain & Efficiency vs. Output Power

V_{DD} = 28 V, I_{DQ} = 950 mA, f = 900 MHz



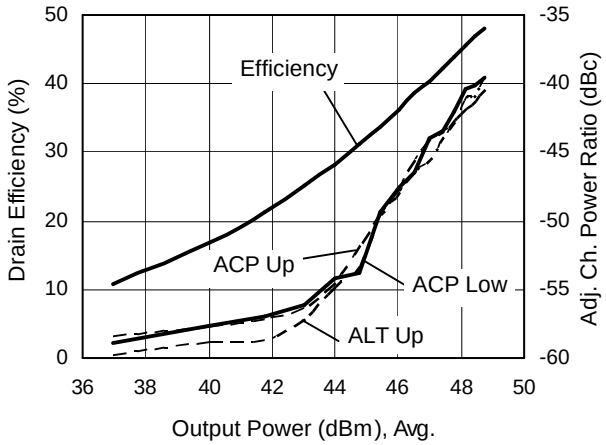
Output Power (at 1 dB Compression) vs. Supply Voltage

I_{DQ} = 950 mA, f = 900 MHz

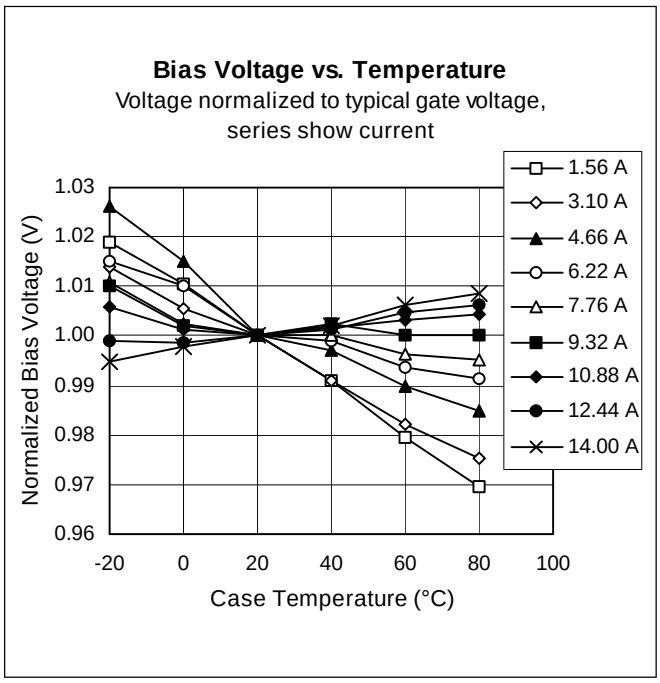


Three-carrier CDMA 2000 Performance

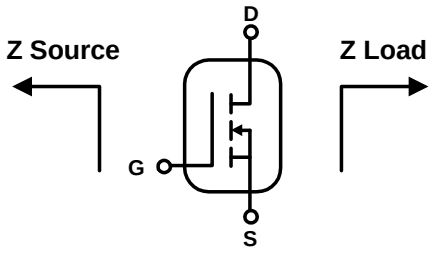
V_{DD} = 28 V, I_{DQ} = 950 mA, f = 900 MHz



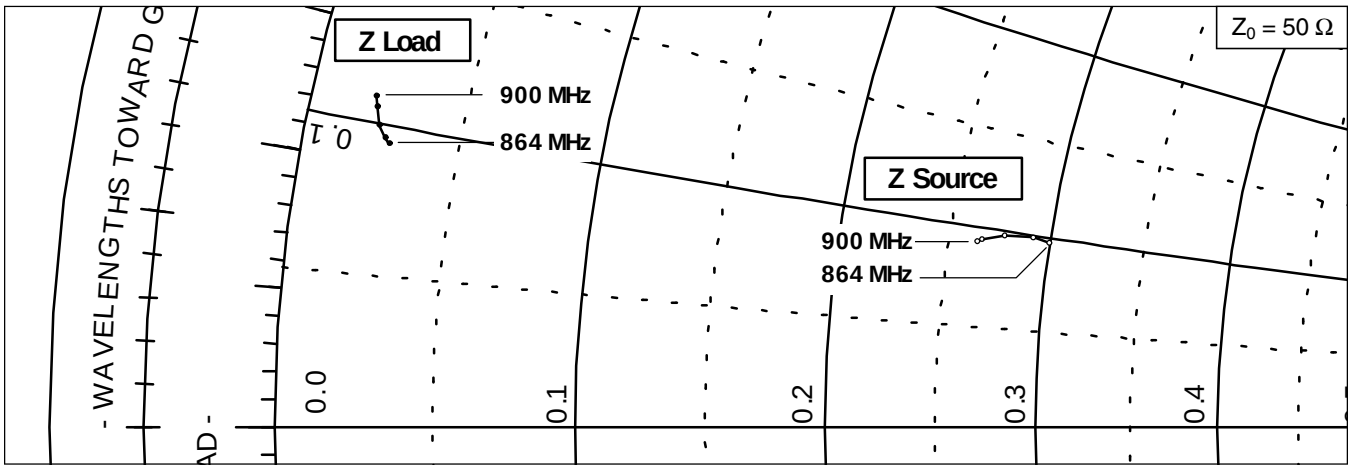
Typical Performance (cont.)



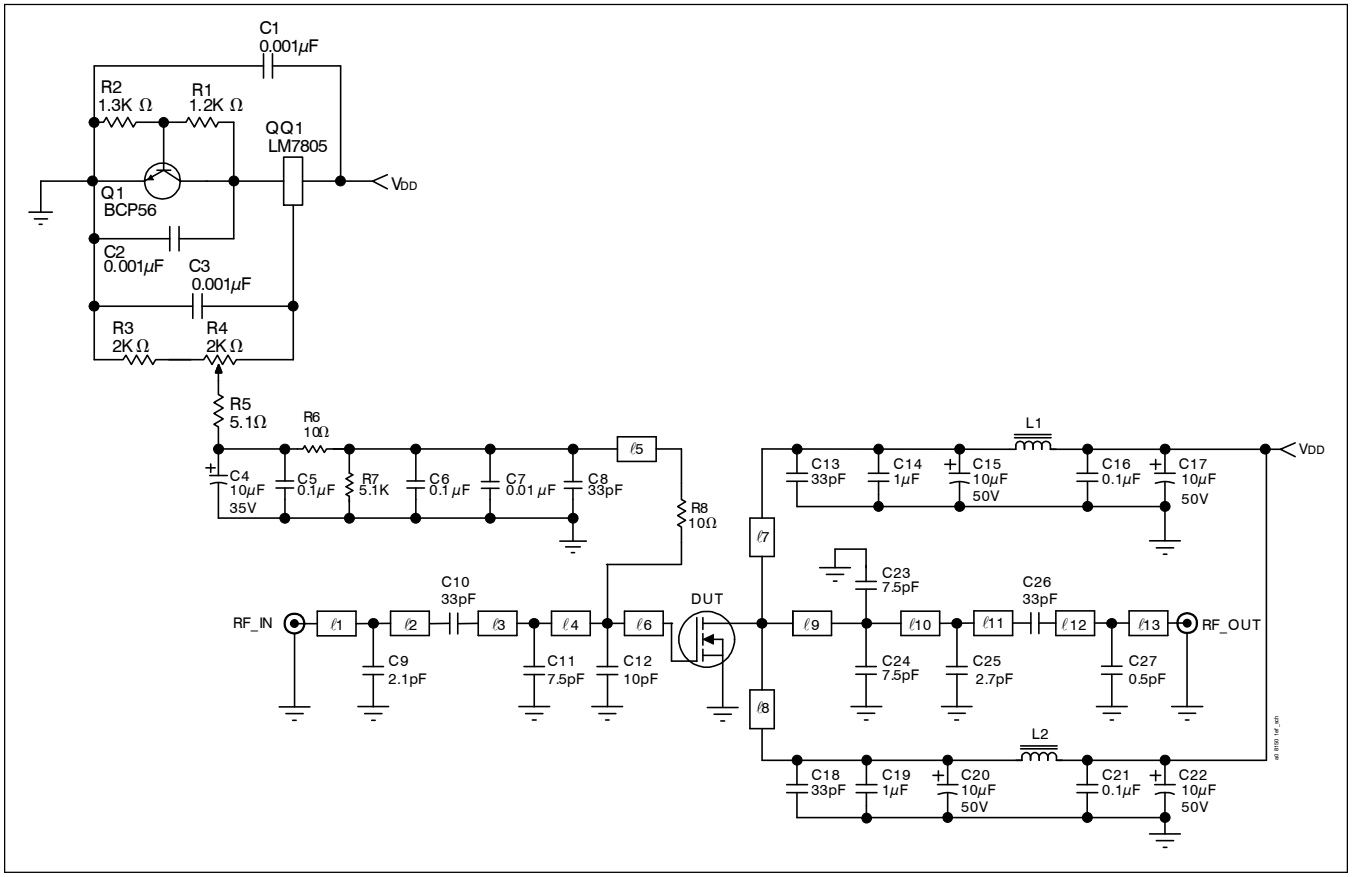
Broadband Circuit Impedance



Frequency	Z Source Ω		Z Load Ω	
MHz	R	jX	R	jX
864	13.20	4.69	1.35	4.73
873	13.30	4.75	1.28	4.80
882	13.85	4.94	1.14	4.99
891	14.59	5.00	1.06	5.27
900	15.01	4.91	1.01	5.43



Reference Circuit



Reference circuit block diagram for ƒ = 900 MHz

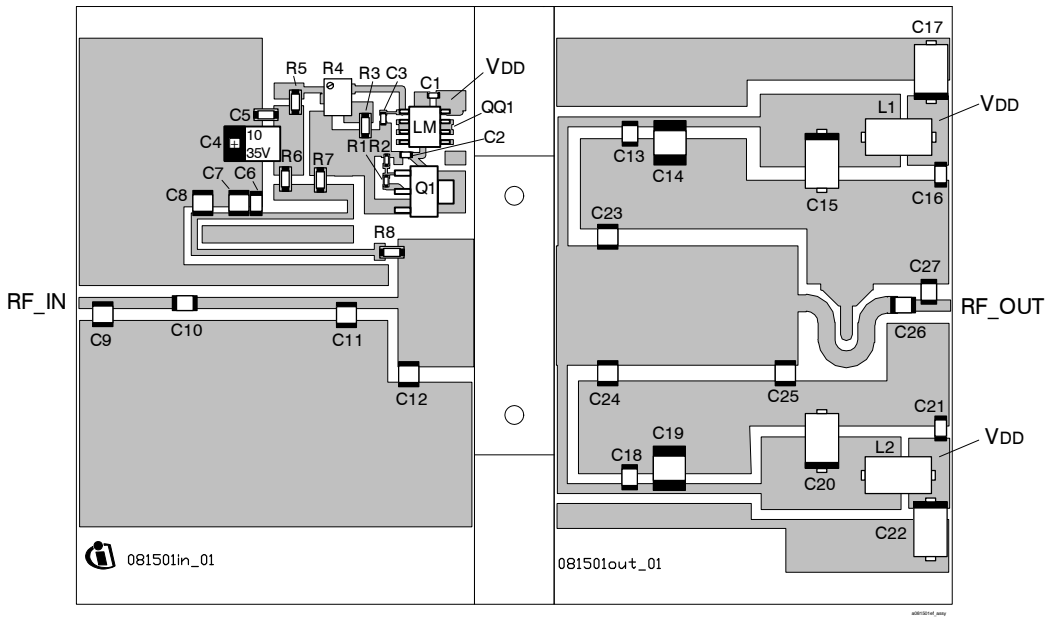
Circuit Assembly Information

DUT	PTFA081501E or PTFA081501F	LDMOS Transistor	
PCB	0.76 mm [.030"] thick, ε_r = 4.5	Rogers TMM4	2 oz. copper

Microstrip	Electrical Characteristics at 900 MHz[1]	Dimensions: L x W (mm)	Dimensions: L x W (in.)
ℓ1	0.016 λ, 50.0 Ω	2.90 x 1.35	0.114 x 0.053
ℓ2	0.053 λ, 50.0 Ω	9.40 x 1.35	0.370 x 0.053
ℓ3	0.102 λ, 50.0 Ω	18.29 x 1.35	0.720 x 0.053
ℓ4	0.045 λ, 50.0 Ω	8.10 x 1.35	0.319 x 0.053
ℓ5	0.153 λ, 68.0 Ω	27.43 x 0.76	1.080 x 0.030
ℓ6	0.058 λ, 7.5 Ω	9.40 x 16.26	0.370 x 0.640
ℓ7, ℓ8	0.125 λ, 50.0 Ω	22.61 x 1.27	0.890 x 0.050
ℓ9	0.036 λ, 7.9 Ω	5.72 x 15.24	0.225 x 0.600
ℓ10	0.141 λ, 7.9 Ω	22.61 x 15.24	0.890 x 0.600
ℓ11	0.149 λ, 38.0 Ω	26.16 x 2.16	1.030 x 0.085
ℓ12, ℓ13	0.013 λ, 50.0 Ω	2.29 x 1.35	0.090 x 0.053

[1]Electrical characteristics are rounded.

Reference Circuit (cont.)



*Reference circuit assembly diagram (not to scale)**

Component	Description	Suggested Manufacturer	P/N or Comment
C1, C2, C3	Capacitor, 0.001 µF	Digi-Key	PCC1772CT-ND
C4	Tantalum capacitor, 10 µF, 35 V	Digi-Key	PCS6106TR-ND
C5, C6, C16, C21	Capacitor, 0.1 µF, 50 V	Digi-Key	P4525-ND
C7	Capacitor, 0.01 µF	Digi-Key	200B 103
C8, C10, C13, C18, C26	Ceramic capacitor, 33 pF	ATC	100B 330
C9	Ceramic capacitor, 2.1 pF	ATC	100B 2R1
C11, C23, C24	Ceramic capacitor, 7.5 pF	ATC	100B 7R5
C12	Ceramic capacitor, 10 pF	ATC	100B 100
C14, C19	Capacitor, 1.0 µF	ATC	920C105
C15, C17, C20, C22	Tantalum capacitor, 10 µF, 50 V	Garrett Electronics	TPS106K050R0400
C25	Ceramic capacitor, 2.7 pF	ATC	100B 2R7
C27	Ceramic capacitor, 0.5 pF	ATC	100B 0R5
L1, L2	Ferrite, 6 mm	Ferroxcube	53/3/4.6-452
Q1	Transistor	Infineon	BCP56
QQ1	Voltage regulator	National Semiconductor	LM7805
R1	Chip resistor, 1.2 k-ohms	Digi-Key	P1.2KGCT-ND
R2	Chip resistor, 1.3 k-ohms	Digi-Key	P1.3KGCT-ND
R3	Chip resistor, 2 k-ohms	Digi-Key	P2KECT-ND
R4	Potentiometer, 2 k-ohms	Digi-Key	3224W-202ETR-ND
R5, R7	Chip resistor, 5.1 k-ohms	Digi-Key	P5.1KECT-ND
R6, R8	Chip resistor, 10 ohms	Digi-Key	P10ECT-ND

**Gerber Files for this circuit available on request*

Package Outline Specifications

Package H-30248-2

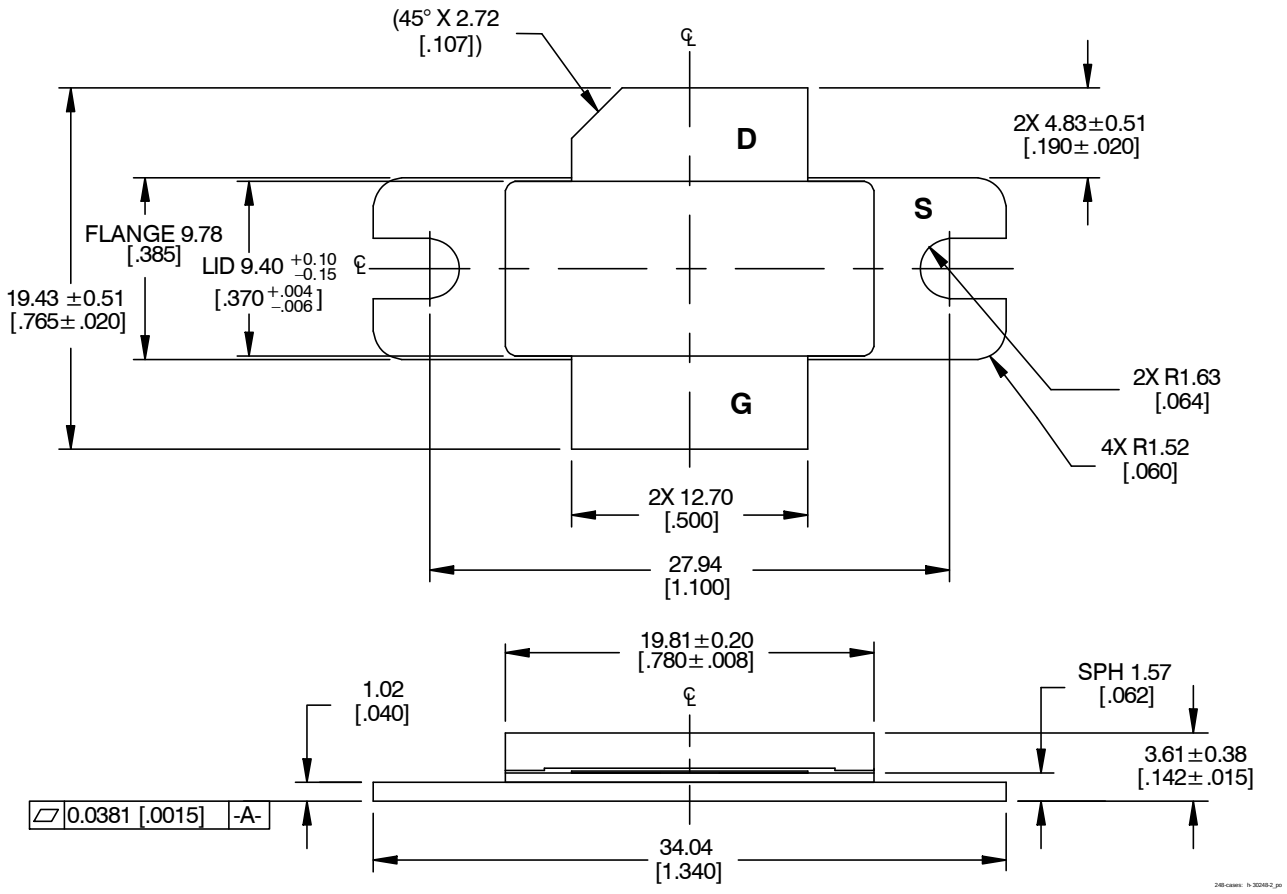


Diagram Notes:

1. Lead thickness: 0.10 +0.051/–0.025 [.004 +.002/–.001].
2. All tolerances ± 0.127 [.005] unless specified otherwise.
3. Pins: D = drain, S = source, G = gate.
4. Interpret dimensions and tolerances per ASME Y14.5M-1994.
5. Primary dimensions are mm. Alternate dimensions are inches.
6. Gold plating thickness:
   S - flange: 2.54 micron (min) [100 microinch (min)]
   D, G - leads: 1.14 micron ± 0.38 micron [45 microinch ± 15 microinch]

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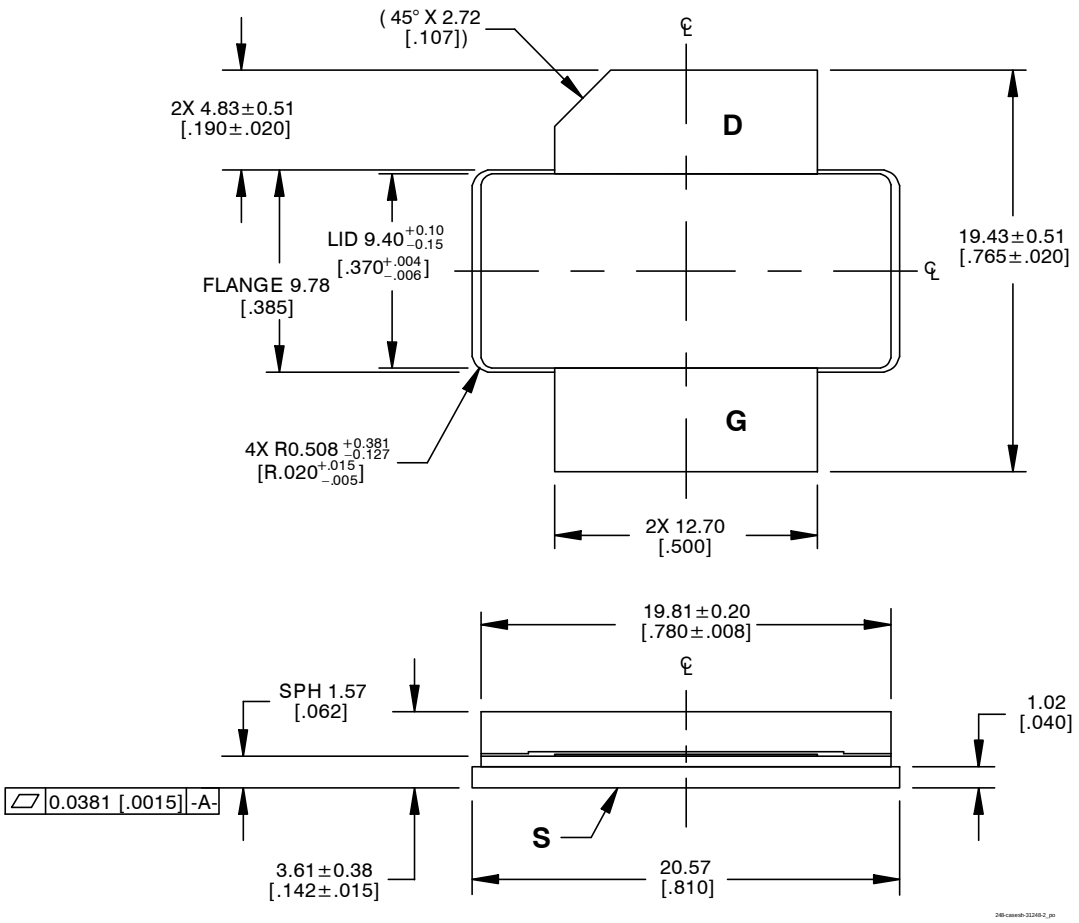
Package Outline Specifications (cont.)

Package H-31248-2



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PTFA081501E/F
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Revision History: 2007-03-09 Data Sheet

Previous Version:	2005-07-20, Data Sheet
Page	Subjects (major changes since last revision)
all	Update Infineon information and logo.
1	Add information about RoHS compliance.
1, 2, 9	Show PTFA081501F as a released products
1, 2, 8, 9	Revise package designations and diagrams.

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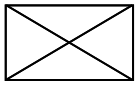

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